Background

There is a class of packages known variously as QFN (for quad flat-pack no-lead) or MLF (for micro lead-frame) that is being employed on printed circuit boards in rapidly increasing quantities. The connection between the component and the board is basically a butt joint between a metalized pad on the bottom of the package and a pad on the board. Inspecting the solder joints on these packages presents a challenge for the 5DX. This is primarily due to the fact that there is no consistent toe or side fillet for these joints. For details see IPC-610D, Section 8.2.13, "Plastic Quad Flat Pack – No Leads (PQFN)". There is also frequently a large pad under the package that is used primarily to transfer heat away from the device. Figure 1 shows a typical x-ray image of a QFN. The 5DX does not currently have an algorithm family specifically designed to test these packages. Several algorithm families have been tried and two, Connector and FlipChip, appear to give good results on the peripheral leads, although the defect spectrum for this joint type is not well understood. The following is a description of the use of FlipChip.

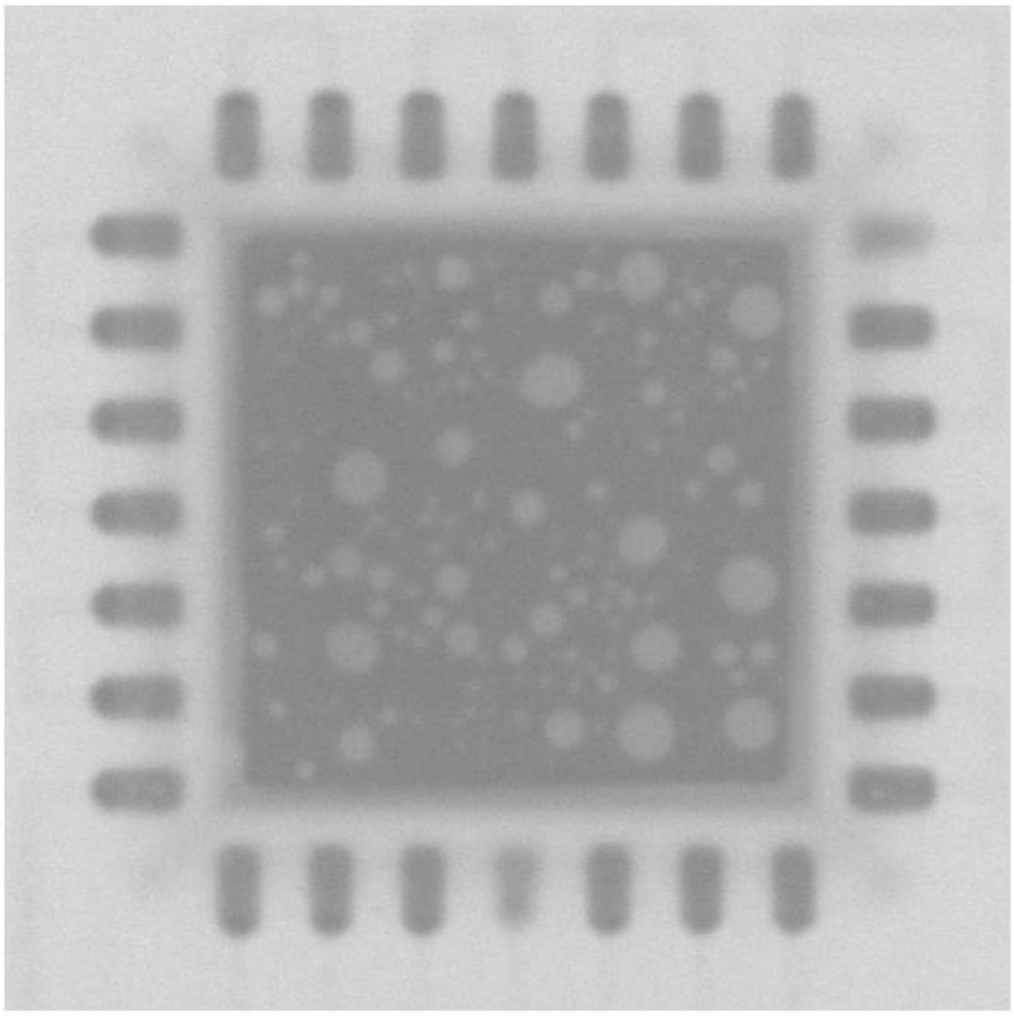

Figure 1. Joints at the top of the right hand column and in the middle of the bottom row are insufficient /open.

Test Strategy

QFNs are available in a wide range of pitches and lead counts. QFNs are tested more reliably using somewhat smaller FOVs than recommended for other package types. 19.7 mil (0.5mm) packages are best tested at a 400 FOV. Larger pitches up to 31.5 mils (0.8mm) are best tested at a 650 FOV. The slice height should be set to the same as used for most other surface mount packages, normally PAD.
There are three different types of defects of primary concern while tuning this algorithm, insufficient, missing and short. Since unreflowed joints, joints with poor wetting, and acceptable joints can be of the same size and shape, testing for "opens" is not reliable. However, the two surfaces to be soldered are in close proximity. There appears to be little chance for solder to be present and to have an open joint. While it is important to catch every missing device, creating a defect call for each pin on a missing device may result in unacceptable false call levels. Typically most but not all pins on a missing device are called.

Algorithm Setup Notes

As for most joint types, proper focus is very important. It may be advisable to set auto-board thickness points to keep the QFNs on the bottom side in focus.

Threshold settings to be aware of:

SPC

Basic

CONTOUR_FRAC
Default is 0.5, but frequently results are better if this value is reduced to about 0.3. The goal here is to have the contour closely follow the edge of the solder.

Additional

USE_CAD
Some subtypes show better results by using 1, "USE_CAD", instead of the default of 0, use nominal.

Short

For many QFNs it may be preferable to set the Region Shape to Rectangular so that there is no overlap with neighboring pads. Thresholds should be set as tight as possible without introducing false calls. The recommendation is to start with thickness thresholds set to 1 mil and increase as necessary.

Thickness thresholds	1-2
Maximum Short Length	1-2

Insufficient

Thresholds need to be tuned for individual applications. The following values are examples:

MIN_DIAMETER_PCT	50 - 60
PAD_REJECT_PCT	80 - 90

Shape

Note: The MIN_PCT_ACROSS threshold should be ignored. It is actually being compared to the Insufficient Width Along measurement.

MIN_PCT_ALONG 65

Defect Analyzer effect.

This particular algorithm is probably more accurate with Defect Analyzer than without it. The reason for this is that if a joint is out of focus the contour fraction collapses and measurements are reported as zero. Defect Analyzer tests at other Z heights. If the image is in reasonable focus and if there is solder present, a good contour is generated. Very rarely on FPGullwing devices testing at other Z heights on a poor joint results in a higher open signal (if some of the solder has wicked up the lead). With FlipChip, because of the lack of that type of open and hence an open signal test, there is less of a chance that Defect Analyzer will create an escape.

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